CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method, comprising:

defining a void in a sacrificial layer proximate to an active layer with a first etching substance reactive with the sacrificial layer, wherein the first etching substance comprises a mixture of H_2SO_4, H_2O_2, and H_2O;

forming an overgrowth layer in the void and over portions of the sacrificial layer adjacent to the void, wherein the overgrowth layer comprises one of InP or AlGaAs;

defining a ridge section in the overgrowth layer with a second etching substance reactive with the overgrowth layer and substantially non-reactive with the sacrificial layer, wherein the second etching substance comprises a mixture of hydrochloric acid (HCl) and phosphoric acid (H_3PO_4); and

removing portions of the sacrificial layer to define a shank section in the overgrowth layer under the ridge section, the ridge section having a greater lateral dimension than the shank section to reduce electrical resistance between the active layer and electrical interconnects to be electrically coupled to the ridge section.

2. (Cancelled)

3. (Previously Presented) The method of claim 1, further comprising forming an etch stop layer between the active layer and the sacrificial layer, the etch stop layer being non-reactive with the first etching substance.

4. (Cancelled)

5. (Previously Presented) The method of claim 1 wherein removing portions of the sacrificial layer to define the shank section in the overgrowth layer comprises etching away the portions of the sacrificial layer with the first etching substance.

6. (Original) The method of claim 1, further comprising forming a planarization layer around the shank section and the ridge section of the overgrowth layer, the planarization layer comprising a polymer.

7. (Original) The method of claim 6, further comprising forming a conductive contact on top of the ridge section, the conductive contact to couple the electrical interconnects to the ridge section.

8. (Previously Presented) The method of claim 1 wherein the overgrowth layer comprises a P-doped semiconductor material and the active layer comprises an intrinsic semiconductor material.

9. (Previously Presented) The method of claim 8 wherein the intrinsic semiconductor comprises one of InGaAsP, InGaAs, and or GaAs.

10. (Cancelled)

11. (Original) The method of claim 1 wherein the ridge and shank sections of the overgrowth layer form a substantially T-shaped ridge structure.

Claims 12-30 (cancelled).

31. (Previously Presented) The method of claim 8, further comprising forming the sacrificial layer over an N-doped substrate layer, wherein the shank section of the overgrowth layer, the active layer, and the N-doped substrate layer form a P-I-N junction.

32. (Previously Presented) A method, comprising:

defining a void in a sacrificial layer proximate to an active layer with a first etching substance reactive with the sacrificial layer;

forming an overgrowth layer in the void and over portions of the sacrificial layer adjacent to the void;

defining a ridge section in the overgrowth layer with a second etching substance reactive with the overgrowth layer and substantially non-reactive with the sacrificial layer; and

removing portions of the sacrificial layer to define a shank section in the overgrowth layer under the ridge section, the ridge section having a greater lateral dimension than the shank section to reduce electrical resistance between the active layer and electrical interconnects to be electrically coupled to the ridge section.

33. (Previously Presented) The method of claim 32 wherein defining the void in the sacrificial layer comprises etching the sacrificial layer.

34. (Previously Presented) The method of claim 32, further comprising forming an etch stop layer between the active layer and the sacrificial layer, the etch stop layer being non-reactive with the first etching substance.

35. (Currently Amended) The method of claim [[34]] 32 wherein removing portions of the sacrificial layer to define the shank section in the overgrowth layer comprises etching away the portions of the sacrificial layer with the first etching substance.

36. (Previously Presented) The method of claim 32, further comprising forming a planarization layer around the shank section and the ridge section of the overgrowth layer, the planarization layer comprising a polymer.

37. (Previously Presented) The method of claim 36, further comprising forming a conductive contact on top of the ridge section, the conductive contact to couple the electrical interconnects to the ridge section.

38. (Previously Presented) The method of claim 32 wherein the overgrowth layer comprises a P-type semiconductor material and the active layer comprises an intrinsic semiconductor material.

39. (Previously Presented) The method of claim 38 wherein the P-type semiconductor material comprises one of InP and AlGaAs, and wherein the intrinsic semiconductor comprises one of InGaAsP, InGaAs, and GaAs.

40. (Previously Presented) The method of claim 39 wherein the first etching substance comprises a mixture of at least two of H_2SO_4, H_2O_2, and H_2O, and wherein the second etching substance comprises a mixture of hydrochloric acid (HCl) and phosphoric acid (H_3PO_4).

41. (Previously Presented) The method of claim 32 wherein the ridge and shank sections of the overgrowth layer form a substantially T-shaped ridge structure.

42. (New) A method, comprising:

defining a void in a sacrificial layer proximate to an active layer with a first etching substance reactive with the sacrificial layer;

forming an overgrowth layer in the void and over portions of the sacrificial layer adjacent to the void;

defining a ridge section in the overgrowth layer with a second etching substance reactive with the overgrowth layer and substantially non-reactive with the sacrificial layer;

removing portions of the sacrificial layer to define a shank section in the overgrowth layer under the ridge section, the ridge section having a greater lateral

dimension than the shank section to reduce electrical resistance between the active layer and electrical interconnects to be electrically coupled to the ridge section; and

forming a planarization layer around the shank section and the ridge section of the overgrowth layer, the planarization layer comprising a polymer.

43. (New) The method of claim 42, further comprising forming an etch stop layer between the active layer and the sacrificial layer, the etch stop layer being non-reactive with the first etching substance.

44. (New) The method of claim 43 wherein removing portions of the sacrificial layer to define the shank section in the overgrowth layer comprises etching away the portions of the sacrificial layer with the first etching substance.

45. (New) The method of claim 42, further comprising forming a conductive contact on top of the ridge section, the conductive contact to couple the electrical interconnects to the ridge section.

46. (New) The method of claim 42 wherein the overgrowth layer comprises a P-type semiconductor material and the active layer comprises an intrinsic semiconductor material.

47. (New) The method of claim 42 wherein the ridge and shank sections of the overgrowth layer form a substantially T-shaped ridge structure.